Remarks/Arguments

There are no amendments to the specification or the drawings hereinabove.

Claims 1-25 remain in this application. Claims 1-3, 6, 8, 9, 11, and 21-25 are rejected. Claims 4, 5, 7 and 10 are objected to. Herein, Claims 1, 9 and 11 have been amended. Reconsideration is respectfully requested.

Claim 1 is amended to correct a minor typographical omission of the preposition 'of' in the claim as originally filed. No new matter is added. Entry of the amendment is respectfully requested.

The Examiner rejected Claims 9 and 11 under 35 U.S.C. 112, second paragraph. In particular, the Examiner contended that there is insufficient antecedent basis for "the mode select input" recited in Claim 9 and for "the pull-up array transistors" recited in Claim 11. Applicant appreciates the Examiner's thorough review of the claims.

Applicant has amended Claims 9 and 11 hereinabove to provide proper antecedent basis for each of the elements recited therein, as required by the Examiner. Specifically, Claim 9 is amended to include "further comprising: a mode select input; and a set of selection inputs" prior to the 'wherein' clause, as originally filed. In addition, the amended Claim 9 also includes several other minor grammatical changes necessitated by the amendment. Claim 11 is amended to depend from Claim 7 instead of from Claim 8, as originally filed. Applicant submits that the amendments to Claims 9 and 11 provide proper antecedent basis and do not add new matter. Entry of the amendments and reconsideration of the rejections are respectfully requested.

The Examiner rejected Claims 1, 2 and 6 under 35 U.S.C. 102(e) as being anticipated by Marr, U.S. Patent No. 6,496,422 (hereinafter 'Marr').

Applicant respectfully traverses the rejection of Claims 1, 2 and 6 in view of Marr on the grounds that the Examiner failed to establish a *prima facie* case of anticipation with respect to Marr. In particular, Applicant submits that Marr fails to disclose, explicitly or implicitly, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)) and/or fails to disclose the claimed elements "arranged as in the claim" (*Lindemann*

Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)) as required by the Federal Circuit for *prima facie* anticipation under 35 U.S.C. 102.

Regarding Claim 1, the Examiner contended, "Fig. 4 of Marr discloses a bias generator [42] for testing a static random access memory SRAM [36] comprising: means [45] for adjusting a set of available magnitudes of a bias voltage output signal at an output the bias generator (connection of 44 of 46. See Col. 4 lines 41-50) using metal programming (Col. 5 lines 5-11)".

Marr discloses a memory structure utilizing four transistor load less memory cells and a bias generator therefor. In particular, Marr discloses, "a current-mirror-based generator for a load less four transistor SRAM" and "methods of controlling or modifying the current conducted by the access transistors of such an SRAM" (Abstract, lines 1-4, Marr). As described by Marr, the disclosed bias generator "may be thought of as an adjustable temperature coefficient, bias generator that references, via a current mirror, a reference bank of SRAM cells" (Abstract, lines 5-7, Marr). Furthermore, Marr discloses that the disclosed bias generator "compensates for both process variations and temperature variations" (Abstract, lines 16-17, Marr).

Regarding the bias generator, Marr discloses, "[t]he bias generator 42 is comprised of bank of transistors 44 connected in parallel with each other and connected in series with a temperature dependent constant current source 46" (Col. 4, lines 23-26, Marr). Furthermore, Marr discloses, "[t]he temperature dependent constant current source may receive inputs from a programmable device 45", which may contain "laser programmable devices, fuses, or antifuses" (Col. 5, lines 5-8). At Col 4, lines 41-50, relied upon by the Examiner, Marr discloses, "the current source 46 [of the bias generator 42] may be constructed using any known techniques which provide a temperature dependent constant current source". Additionally, Marr discloses, "for each value of current produced by the temperature dependent constant current source 46, a different voltage drop across the gate and source terminals of the transistors 44 is produced".

However, contrary to that contended by the Examiner, Marr fails to disclose that recited in Applicant's Claim 1. For example, Marr does not disclose "means for

adjusting ... using ***metal programming***", as recited in Applicant's Claim 1 (***emphasis*** added). For example, no portion of the bias generator 42 disclosed by Marr employs ***metal programming***. In fact, Marr never mentions ***metal programming*** of any device or circuit element or in any context whatsoever, contrary to that contended by the Examiner.

Furthermore, the term 'metal programming' is clearly defined in Applicant's specification as "establishing and/or removing connections in an integrated circuit (IC) by changing a routing pattern of an interconnect layer, preferably a final or 'top' interconnect layer, of the IC during circuit fabrication" (Page 6, lines 10-13, Applicant's specification as filed). In addition to being clearly defined by Applicant, the definition and subsequent usage of the term 'metal programming' by Applicant are consistent with a conventional understanding of the term in the art.

Marr does refer to "a laser trimmable device, fuses, or antifuses" in at least two places (Col. 5, lines 7-8, lines 46-47, Marr). However, in both instances, Marr further discloses that adjustment or control afforded by the devices occurs or is implemented "post fabrication" (Col. 5, line 11, lines 49-50). Metal programming, as defined by Applicant, occurs or is implemented ***during circuit fabrication***. As such, Marr's reference to 'post fabrication' explicitly precludes the use of metal programming for the devices. Therefore, neither at Col. 5, lines 5-11, relied upon by the Examiner, nor anywhere else in that disclosed by Marr is metal programming disclosed, or even suggested, contrary to that contended by the Examiner.

Furthermore, Marr fails to disclose or suggest a "bias generator", as defined by Applicant's specification and recited in Claim 1. In particular, the 'bias generator' claimed by Applicant provides a "bias voltage output signal" to a write driver of SRAM for implementing weak write testing thereof (see for example, Page 5, lines 5-19, Applicant's specification, as filed). Specifically, the bias voltage output signal is applied to a gate of 'weak' NFET of the write driver.

By contrast, Marr discloses a bias generator 42 that is connected to "word lines WL1-WL4 through a transistor pair 52" (Col. 5, lines 19-20, Fig. 5, Marr). As is clearly illustrated in Fig. 5 of Marr, each transistor pair 52 comprises a PMOS and an NMOS transistor wherein the PMOS transistor is "connected between the bias

generator 42 and a word line, e.g., WL1" while the NMOS transistor is "connected between the word line, e.g., WL1, and ground" (Col. 5, lines 22-25, Marr). The word line 'WL' , in turn, is connected to a gate of each of the access transistors 38, 40, in the memory cell 36. The access transistors 38, 40 control read/write access to the memory cell (i.e., cell 36) while the transistor pair 52 serves as a driver/buffer for the word line WL and is "responsive to a word line select signal, e.g., Sel WL1" (Col. 5, lines 25-26, Marr). The bias generator 42 connects to a source of a PMOS transistor and is "used to control conduction characteristics of the access transistors 38 and 40" (Col. 4, lines 62-63, Marr). Hence, the bias generator 42 disclosed by Marr is distinctly different from and used in a different manner than that claimed by Applicant.

Moreover, Marr discloses applying the "bias generator 42" to a "load-less 4 transistor SRAM cell 36" (see Fig. 4, Col. 4, lines 9-20). Weak write testing is not applicable to 4-transistor SRAM cells as is well-known by those skilled in the art. Therefore, for at least these reasons, Marr does not and respectfully cannot disclose each element recited in Applicant's Claim 1.

Regarding Claim 2, the Examiner contended, "Fig. 4 of Marr discloses wherein the bias voltage output signal [48] biases a gate of a weak write pull-down transistor [26] of a write driver [WL] in the SRAM [36] with a target magnitude predetermined (Col. 4 lines 47-51) for the SRAM [36]."

Contrary to the Examiner's contention, Marr fails to disclose or even suggest that recited in Applicant's Claim 2. For example, Marr neither discloses nor suggests weak write testing since such testing is not applicable to the disclosed load-less 4-transistor SRAM cell. Instead, Marr discloses and is concerned with satisfying "the simultaneous constraints of yield, sense amp margin, and load current even during cold-data retention testing or burn-in" (Col. 3, lines 24-26, Marr). One skilled in the art would readily recognize a distinct difference between such a concern and weak write testing (i.e., that uses 'a weak write pull-down transistor' and 'a write driver'), as claimed by Applicant.

Furthermore, transistor 26 disclosed by Marr neither is a 'weak write pull-down transistor' nor can it be employed as one. In particular, as is known in the art,

to implement weak write testing, a pair of pull-down transistors is employed in parallel in a write driver (see for example, Weiss et al., U.S. Patent No. 6,192,001, incorporated by reference in Applicant's specification as filed). A first transistor of the pair is the weak write pull-down transistor that "modifies a level of an output signal of the write driver" when in weak write test mode (WWTM) while the second transistor of the pair is a bypass pull-down transistor that "bypasses the first transistor thereby facilitating a normal or strong write output signal to be produced by the write driver when not in WWTM" (Page 2, lines 6-9, Applicant's specification).

In addition, "the weak write pull-down transistor must be big or strong enough to insure that the WWTM write driver output signal adequately exercises the memory cells of the SRAM, allowing for reliable detection of defective memory cells" and simultaneously, "the weak write pull-down transistor must be small or weak enough such that the WWTM write driver output signal is not capable of overwriting data in healthy memory cells thereby producing false detection of defects" (Page 2, lines 11-17, Applicant's specification).

On the other hand, according to Marr, transistor 26 is an NMOS pull-down transistor of a "storage circuit 20" or of a "load-less 4 transistor SRAM cell 36" and not part of a write driver. For that matter, transistor 26 is not even part of the bias generator 42 disclosed by Marr (see Figs. 1 and 2, and Col. 1, lines 32-33, or Figs. 3 and 4, and Col. 4, lines 19-20, Marr). Thus, transistor 26 is not and simply cannot be the "weak write pull-down transistor" recited in Applicant's Claim 2. Moreover, nowhere else in that disclosed by Marr is there to be found a transistor that has the characteristics recognized in the art as necessary for being a weak write pull-down transistor.

Furthermore, contrary to that contended by the Examiner, a 'WL' or 'word line', such as that disclosed by Marr, is not a "write driver". By convention and as employed by Applicant, the write driver is connected to and provides drive signals to BIT lines of the SRAM, as mentioned hereinabove.

In contrast, the word line WL disclosed by Marr is a word select line used to select memory cells for reading or writing by way of the access transistors 38 and 40. Marr distinguishes the word line WL from the BIT lines $D/\overline{D}$ that carry data.

Hence, the Examiner respectfully is in error by equating the word line WL of Marr with the "write driver" recited in Applicant's Claim 2.

Additionally, according to Marr, "[t]he bias generator 42 may be coupled to each of the word lines WL1-WL4 through a transistor pair 52" (Col. 5, lines 18-20, Marr). As such, Marr cannot disclose "the bias voltage output signal biases a gate of a weak write pull-down transistor of a write driver in the SRAM", as recited, in part, in Applicant's Claim 2, since the bias generator 42 of Marr is explicitly connected to word lines WL1-WL4 and not to a portion of a write driver of the disclosed SRAM. Thus for at least the reasons cited hereinabove, Marr does not, and respectfully cannot disclose or even suggest that recited in Applicant's Claim 2.

Regarding independent Claim 6, the Examiner contended, "Fig. 5 of Marr discloses a bias generator [42] for testing (Col. 4 lines 44-47) of a static random access memory SRAM [36] comprising: a metal programmable transistor [58] that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed (Col. 5 lines 39-50)".

Contrary to that contended by the Examiner, Marr neither discloses nor suggests that recited in Applicant's Claim 6. For example, Marr fails to disclose a metal programmable transistor or metal programming thereof. Instead, "transistor 58", as disclosed by Marr, is simply p-type or PMOS transistor (see Fig. 5, Marr). According to Marr, "[t]o provide a particular voltage for a test mode, a voltage source 56 may be coupled to the global bus 54 through a transistor 58" (Col. 5, lines 39-41, Marr). Marr never suggests that transistor 58 is or could be metal programmable. Moreover, as discussed hereinabove, Marr fails to disclose or even suggest using metal programming at all, so Marr cannot disclose a metal programmable transistor.

In addition, Marr specifically provides for the voltage source 56 "outputting different voltages depending upon one or more control signals 60" and discloses that the "[v]oltage source 56 may include a constant current source as well as a laser trimmable device, fuses, or antifuses ... giving the manufacturer some degree of control over the voltage(s) produced by the voltage source 56 post fabrication" (Col. 5, lines 41-43 and lines 48-50, Marr). As such, there is no suggestion that a metal programmable transistor might be used to implement 'transistor 58' since Marr

teaches adjusting the outputs of voltage source 56 itself. Marr does not need or recognize a need for metal programming (or any other form adjustability for that matter) of transistor 58.

Given that Marr fails to disclose using metal programming and a metal programmed transistor, Marr cannot disclose "a metal programmed transistor that adjusts a set ... when metal programmed", as recited in Applicant's Claim 6. Moreover, as discussed hereinabove, Marr even fails to disclose a "bias generator", as recited in Applicant's Claim 6. Thus for at least the reason detailed hereinabove, Marr does not, and respectfully cannot, disclose or even suggest each element recited in Applicant's Claim 6.

It is respectfully submitted that the Examiner has failed to establish a *prima facie* case of anticipation of Claim 1, 2 and 6 with respect to Marr. In particular, the Examiner failed to show that there is "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention" as required by the Federal Circuit. *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991). In addition, Claim 2 is dependent from Claim 1. As such, having failed to establish *prima facie* anticipation of Claim 1, the Examiner has similarly failed to establish *prima facie* anticipation of respective Claim 2. This is so independently of the exclusive features recited in Claim 2, Therefore, the rejection of Claims 1, 2 and 6 under 35 U.S.C. 102(e) with respect to Marr is unsupported by facts in evidence and respectfully must be withdrawn.

The Examiner rejected Claims 1, 3, 6, 8 and 21-25 under 35 U.S.C. 102(e) as being anticipated by Sher et al., U.S. Patent No. 6,756,805 (hereinafter 'Sher et al.').

Applicant respectfully traverses the rejection of Claims 1, 3, 6, 8 and 21-25 in view of Sher et al. on the grounds that the Examiner failed to establish a *prima facie* case of anticipation with respect to Sher et al. In particular, Applicant submits that Sher et al. fail to disclose, explicitly or implicitly, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, cited *supra*) and/or do not disclose the claimed elements "arranged as in the claim" (*Lindemann*

Maschinenfabrik GmbH v. American Hoist & Derrick Co., cited *supra*), as required by the Federal Circuit for *prima facie* anticipation under 35 U.S.C. 102.

Regarding independent Claim 1, the Examiner contended, "Fig. 4 of Sher et al. discloses a bias generator for testing a static random access memory SRAM (intended of use) comprising: means (Fig. 4 [HIGHVBB1, HIGHVBB2, LOWVBB1, LOWVBB2, NORMVBB]) for adjusting a set of available magnitudes of a bias voltage output signal at an output the bias generator (Col. 9 lines 43-58) using metal programming (Fig. 6, Fig. 7)".

Contrary to that contended by the Examiner, Sher et al. do not disclose or even suggest that recited in Applicant's Claim 1. For example, Sher et al. do not disclose using 'metal programming' or even an equivalent thereof. In particular, Figs. 6 and 7 of Sher et al., relied upon by the Examiner, do not illustrate or even imply that 'metal programming' is used.

Instead, according to Sher et al., "FIG. 6 is a schematic circuit diagram of an anti-fuse circuit for providing signals for the voltage generating circuit of FIG. 4 for maintaining the voltage at an adjusted level" and "FIG. 7 is a block diagram of logic circuits for producing test signals for the voltage generating circuit of FIG. 4" (Col. 4, lines 14-19). The programmable circuits of Fig. 6 and the NOR/NAND logic circuits of Fig. 7 are employed "to maintain the voltage at a magnitude to which it is adjusted" (Abstract, lines 13-14, Sher et al.). The term 'voltage' refers to voltages HIGHVBB1, HIGHVBB2, LOWVBB1, LOWVBB2, NORMVBB that are adjusted after circuit manufacture, according to Sher et al. Specifically, at Col. 11, lines 29-48, Sher et al. clearly describe programming the programmable circuits (i.e., adjusting the voltages HIGHVBB1, HIGHVBB2, LOWVBB1, LOWVBB2, NORMVB) while the circuit is operating. As such, programming, according to Sher et al., must necessarily occur after circuit manufacture and not during manufacture as would be the case with the art-recognized use of metal programming. Therefore, Sher et al. not only fail to disclose or even suggest using metal programming, but explicitly preclude the use of metal programming to implement the disclosed programmable circuits.

In addition, Sher et al. do not disclose "a bias voltage output signal at an output of the bias generator", as recited in Applicant's Claim 1. In particular,

according to Applicant's specification, the bias generator is connected to a write driver of SRAM for implementing weak write testing thereof (see for example, Page 5, lines 5-19, Applicant's specification, as filed). In addition, as discussed hereinabove, the write driver is connected to and provides drive signals to BIT lines of the SRAM, according to Applicant's specification.

In contrast, Sher et al. disclose a voltage generating circuit that "provides a substrate bias voltage Vbb or wordline bias voltage Vccp" for an IC device or alternatively, "an internal voltage, such as the cellplate or equilibrating voltage DVC2" for a memory circuit (Col. 20, lines 40-43). Nothing in that taught by Sher et al. suggests using the disclosed voltage generator in conjunction with a write driver to drive BIT lines of SRAM. Thus, Sher et al. fail to disclose or suggest either "the bias generator" or the "bias generator output signal", as defined by Applicant's specification and recited in Claim 1.

Moreover, Sher et al. do not disclose or even suggest using 'SRAM' or SRAM testing. On the contrary, with respect to memory circuits, Sher et al. explicitly and exclusively disclose testing dynamic random access memory (DRAM). One skilled in the art would readily recognize a distinct difference between testing DRAM and testing SRAM.

Applicant is unsure what to make of the Examiner's reference to "SRAM (intended of use)" in the stated reason for rejection. It is possible that the Examiner may consider SRAM equivalent to DRAM despite the well-recognized and distinct difference known in the art between SRAM and DRAM. Alternatively or additionally, the Examiner may be asserting that SRAM is somehow inherent in that disclosed by the reference.

However, while the Examiner may allege or assert equivalence or inherency when a single reference lacks explicit disclosure of a missing characteristic or element, the Examiner must provide evidence that the missing characteristic or element is necessarily present in that disclosed by the reference. As stated by the Federal Circuit, , "[t]o serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence ***must make clear that the missing descriptive***

matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991) (***emphasis*** added).

The Examiner has not provided extrinsic evidence of any kind to support "intended of use". As such, without an explicit teaching by Sher et al. that SRAM may be substituted for the disclosed DRAM and in the absence of any evidence that makes clear the presence of the missing matter, the Examiner's reference to "intended of use", as interpreted by the undersigned hereinabove, is respectfully improper. Hence, for at least the reason detailed hereinabove, Sher et al. do not, and respectfully cannot, disclose or even suggest each element recited in Applicant's Claim 1.

Regarding independent Claim 6, the Examiner contended, "Fig. 4 of Sher discloses a bias generator for testing (Col. 8 lines 47-51) of a static random access memory SRAM (intended of use) comprising: a metal programmable transistor (Fig. 6) that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed (Col. 9 lines 43-58).

Contrary to that contended by the Examiner, Sher et al. neither disclose nor suggest that recited in Applicant's Claim 6. For example, Sher et al. fail to disclose either a metal programmable transistor or metal programming thereof.

Instead, Fig. 6 of Sher et al., relied upon by the Examiner, illustrates a programmable circuit. As discussed hereinabove, the programmable circuit according to Sher et al. is clearly programmed after circuit manufacture (see for example, Col. 11, lines 29-48). As such, neither the programmable circuit of Fig. 6 nor any component therein is or can be a metal programmable transistor, which is programmed during manufacture, according to the art-recognized definition of 'metal programming' and according to Applicant's specification (Page 6, lines 10-13, as filed). Additionally, as discussed hereinabove, Sher et al. do not disclose or even suggest 'metal programming' in any form whatsoever. As such, Sher et al. do not and cannot disclose a metal programmable transistor.

Moreover, as discussed hereinabove, Sher et al. fail to disclose or even suggest "the bias generator", as defined by Applicant's specification and recited in Applicant's Claim 6. In fact, Sher et al. even fail to disclose or suggest SRAM or the

testing thereof, as discussed hereinabove. Thus, for at least the reason detailed hereinabove, Sher et al. do not, and respectfully cannot, disclose or even suggest each element recited in Applicant's Claim 6.

Regarding independent Claim 21, the Examiner contended, "Sher et al. discloses a method of modifying a set of available magnitudes of a bias voltage output signal generated by a bias generator comprising (Col. 3 lines 36-52): providing a metal programmable transistor (Fig. 6) in the bias generator (Fig. 4 [HIGHVBB1, HIGHVBB2, LOWVBB1, LOWVBB2, NORMVBB]); and metal programming the metal-programmable transistor (Fig. 6) to connect the transistor to circuitry of the bias generator (Fig. 4), such that a corresponding ON state resistance (Fig. 6 HFS1) of the metal-programmed transistor is combined with an effective ON state resistance (Fig. 7) of the circuitry to modify the available magnitudes of the set (Col. 9 line 43 – Col. 10 line 6).

Contrary to that contended by the Examiner, Sher et al. do not disclose that recited in Applicant's Claim 21. For example, as discussed hereinabove, Sher et al. neither disclose nor suggest a metal programmable transistor or metal programming thereof. Thus, Sher et al. does not and cannot disclose "providing a metal programmable transistor" or "metal programming the metal-programmable transistor", as recited in Applicant's Claim 21. Furthermore, as discussed hereinabove, Sher et al. fail to disclose the "bias generator", as defined in Applicant' specification and recited in Applicant's Claim 21.

Moreover, according to Sher et al., 'HFS1' is a test signal generated by an output of an inverter logic gate of the programmable circuit of Fig. 6 (see for example, Col. 9, line 67 to Col. 10, line 1, Sher et al.). As such, contrary to the Examiner's contention, Sher et al. do not disclose in Fig. 6, by way of HFS1, a "corresponding ON state resistance", as recited in Applicant's Claim 21. In addition, according to Sher et al., the test signal HFS1 is applied to an input of a NOR gate of the NOR/NAND logic circuits of Fig. 7 of Sher et al. (see for example, Col. 11, lines 10-16, Sher et al.). As such, contrary to the Examiner's contention, Sher et al. do not disclose in Fig. 7, combining the "corresponding ON state resistance" with "an effective ON state resistance of the circuitry". Such a contention on the part of the

Examiner regarding the teachings of Sher et al. is incompatible with a conventional understanding of the operation of logic devices, such as inverters and NOR gates, as employed by Sher et al. Therefore, for at least the reason detailed hereinabove, Sher et al. do not and respectfully cannot disclose or even suggest each element recited in Applicant's Claim 21.

It is respectfully submitted that the Examiner has failed to establish a *prima facie* case of anticipation of independent Claims 1, 6 and 21 with respect to Sher et al. In particular, the Examiner failed to show that there is "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention", as required by the Federal Circuit. *Scripps Clinic & Research Found. V. Genentech Inc.*, cited *surpa*).

In addition, Claim 3 is dependent from Claim 1, Claim 8 is dependent from 6, and Claims 22-25 are ultimately dependent from Claim 21. As such, having failed to establish *prima facie* anticipation of Claims 1, 6 and 21, the Examiner has similarly failed to establish *prima facie* anticipation of respective dependent Claims 3, 8, and 21-25. This is so independently of the exclusive features recited in Claims 3, 8, and 22-25, Therefore, the rejection of Claims 1, 3, 6, 8 and 21-25 under 35 U.S.C. 102(e) with respect to Sher et al. is unsupported by the facts in evidence and respectfully must be withdrawn.

The Examiner objected to Claims 4, 5, 7 and 10 as being dependent upon rejected base claims. Applicant appreciates the Examiner's acknowledgement that Claims 4, 5, 7 and 10 would be allowable if rewritten in independent form. However, in light of Applicant's arguments hereinabove, Applicant respectfully submits that Claims 4, 5, 7 and 10 are in allowable form, as originally filed. Thus, Applicant defers rewriting these claims pending Examiner's review of the arguments presented hereinabove.

Applicant appreciates the Examiner's acknowledgement of the allowability of Claims 9 and 11 if rewritten to overcome the rejections under 35 U.S.C. 112, second paragraph. Applicant has amended Claims 9 and 11 to overcome the rejections.

Further, Applicant appreciates the Examiner's allowance of Claims 12-20, as filed.

In summary, Claims 1-25 were pending. Claims 1-3, 6, 8, 9, 11, and 21-25 were rejected, Claims 4, 5, 7, and 10 were objected to, and Claims 12-20 were allowed. Applicant has amended Claims 1, 9 and 11, herein. It is respectfully requested that Claims 1-11 and 21-25 be allowed along with allowed Claims 12-20, and that the application be passed to issue at an early date.

Should the Examiner's action be other than allowance, the undersigned respectfully requests a telephone call from the Examiner to discuss further consideration that would expedite the prosecution of the application. Furthermore, should the Examiner have any questions regarding the above, please contact the undersigned, J. Michael Johnson, Agent for Applicant, at telephone number (775) 849-3085.

Respectfully submitted,
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

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